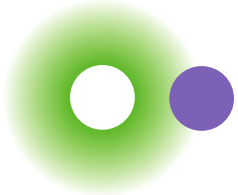

NICTA

The Last Mile
An Empirical Study of
Timing Channels on seL4

David Cock Qian Ge Toby Murray Gernot Heiser

4 November 2014

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seL4
Channels
Experimental Approach
Local Channels
The Cache Channel
Instruction-Based Scheduling
Cache Colouring
New Channels
Remote Channels
Scheduled Delivery
Summary
Outcomes
Ongoing Work

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QUT
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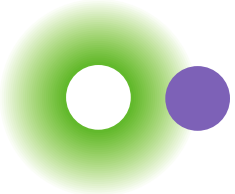

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seL4

seL4 is a verified, high-performance microkernel. We have:

- Proof of **functional correctness**.
- Proof of **authority confinement**.
- Proof of **explicit information-flow control**.
- **WCET** analysis.

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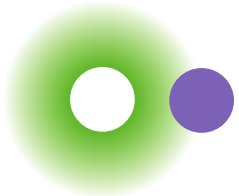

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- Proof of **functional correctness**.
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- **WCET** analysis.

We don't have:

- An comprehensive hardware model.

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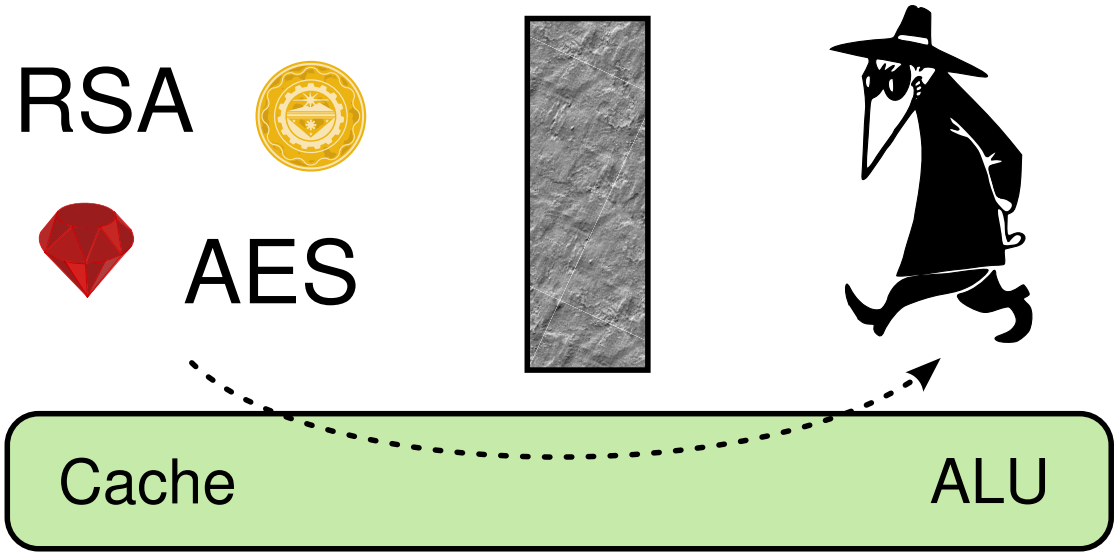
Covert and Side Channels



Unexpected channels invalidate info-flow control.
We can't prove their absence:

- Depend heavily on undocumented chip internals.
- Channels are probabilistic.

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Channels of Interest

Channels we consider

- Can subvert our proof: *Timing channels*.
- Could be fixed with OS techniques e.g. *Cache contention*.
- That can be exploited in software.

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Channels of Interest

Channels we consider

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- Could be fixed with OS techniques e.g. *Cache contention*.
- That can be exploited in software.

Channels we **don't** consider

- Physical attacks e.g. *DPA*.
- Channels already excluded by proof e.g. *Storage channels*.

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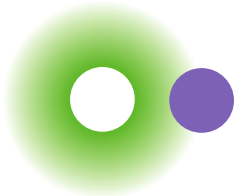

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- The L2 cache channel.
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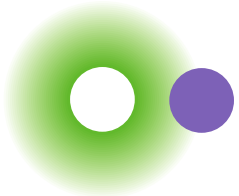

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- Instruction-based scheduling.
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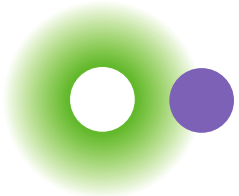

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- Lucky-13 against OpenSSL is our example victim.

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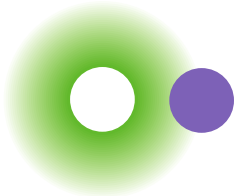

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We also consider countermeasures against **remote, algorithmic** channels:

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- Scheduled delivery is our countermeasure.

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Experimental Platforms

	Core	Date	L2 Cache
iMX.31	ARM1136JF-S (*ARMv6*)	2005	128 KiB
E6550	Conroe (*x86-64*)	2007	4096 KiB
DM3730	Cortex A8 (*ARMv7*)	2010	256 KiB
AM3358	Cortex A8 (*ARMv7*)	2011	256 KiB
iMX.6	Cortex A9 (*ARMv7*)	2011	1024 KiB
Exynos4412	Cortex A9 (*ARMv7*)	2012	1024 KiB

- 7 years and 3 (ARM) core generations.
- 32-fold range of cache sizes.

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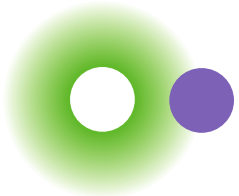
Methodology



- Integrated with nightly regression test.
- Runs each channel with each countermeasure (54 combinations).
- 2,000 hours of data over 12 months, 4.3 GiB.
- Data and analysis tools open source: `http://ssrg.nicta.com.au/projects/TS/timingchannels.pml`

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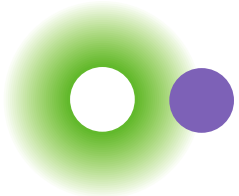

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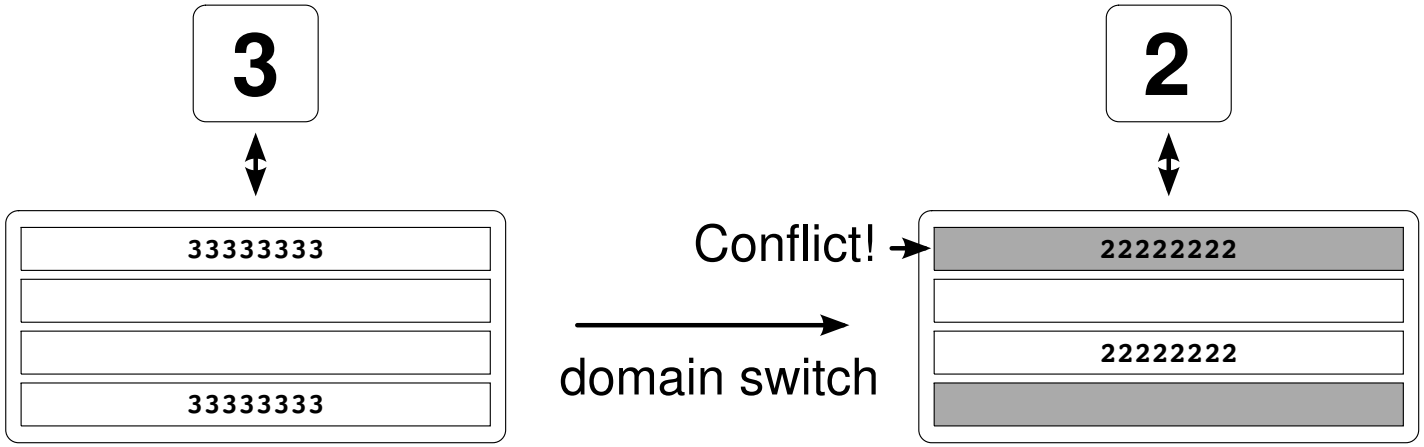
Cache Contention



- If you share a core, you share a cache.
- Hit vs. miss makes a **big** time difference.
- Many published attacks steal keys through the cache.

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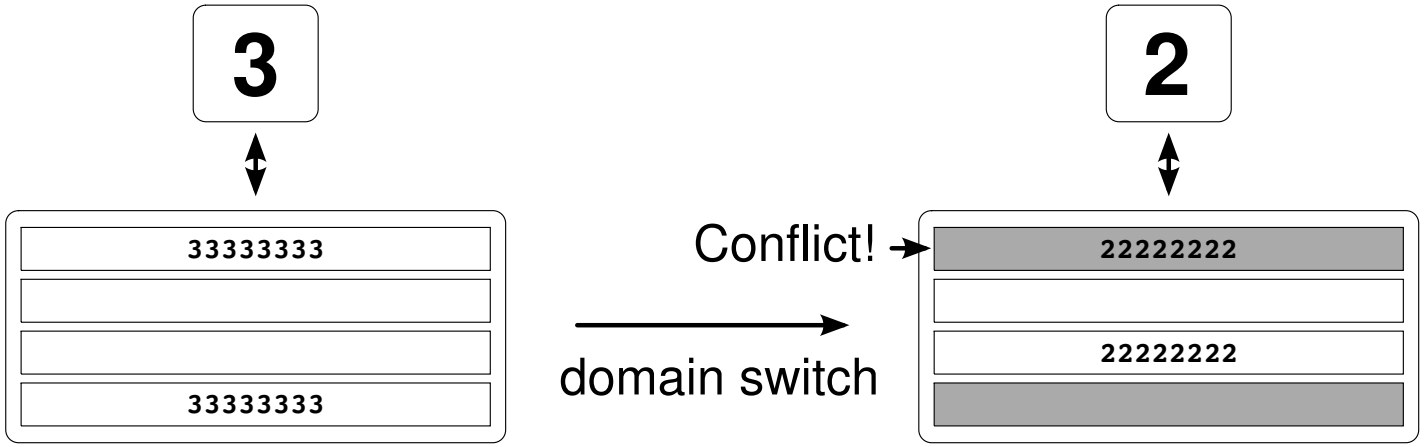

- If you share a core, you share a cache.
- Hit vs. miss makes a **big** time difference.
- Many published attacks steal keys through the cache.
- We can control cache allocation (more shortly).

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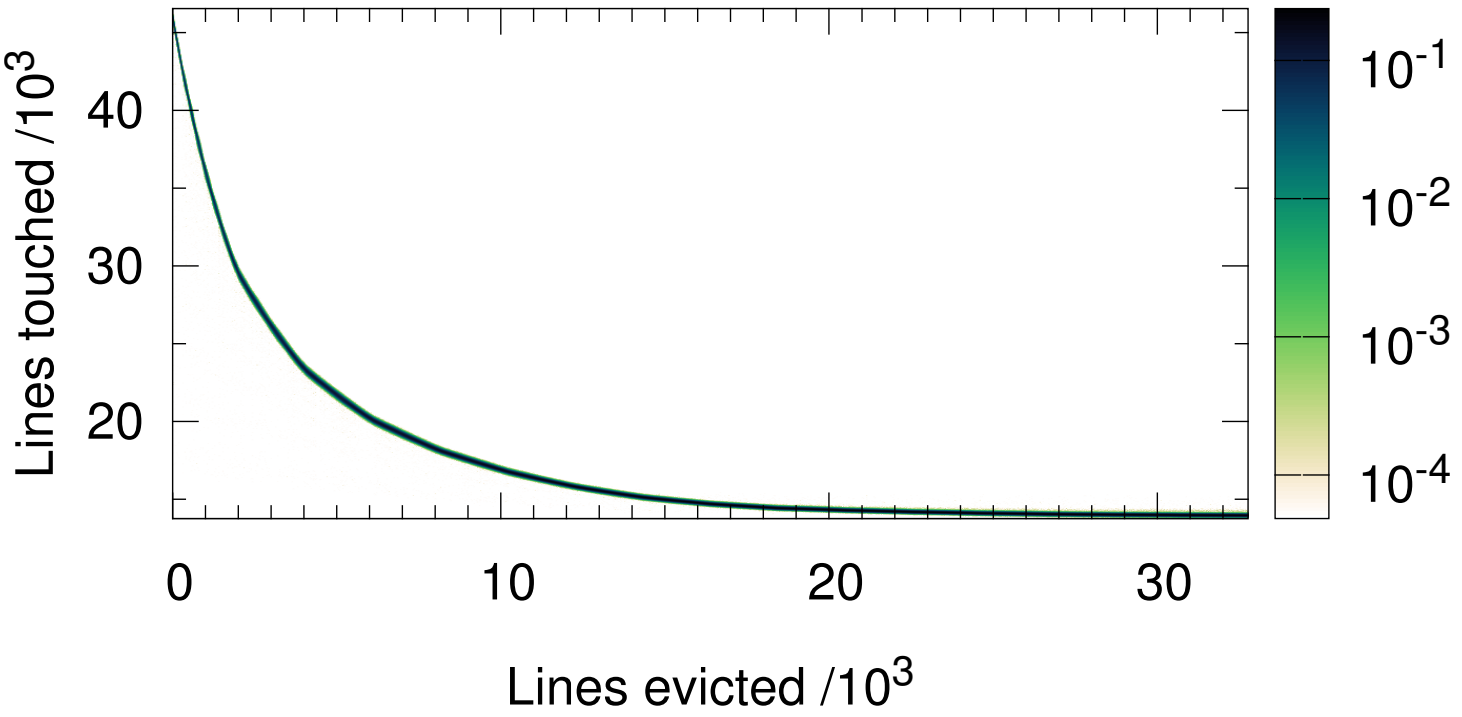
Exynos4412 Cache Channel



- 32,768 cache lines, 1000Hz sample rate (preemption).
- Bandwidth: 2400b/s.
- Baseline for comparison.

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What is Instruction-Based Scheduling (IBS)?

Our example attack used preemption as a clock. If it's tied to progress, the channel should vanish.
This is a form of **deterministic execution**.

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Advantages

- Applies to any channel.
- Simple to implement (18 lines in seL4).

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Disadvantages

- Restrictive — Need to remove **all** clocks.
- Performance counter accuracy critical.

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Works great on older chips (iMX.31), but. . .

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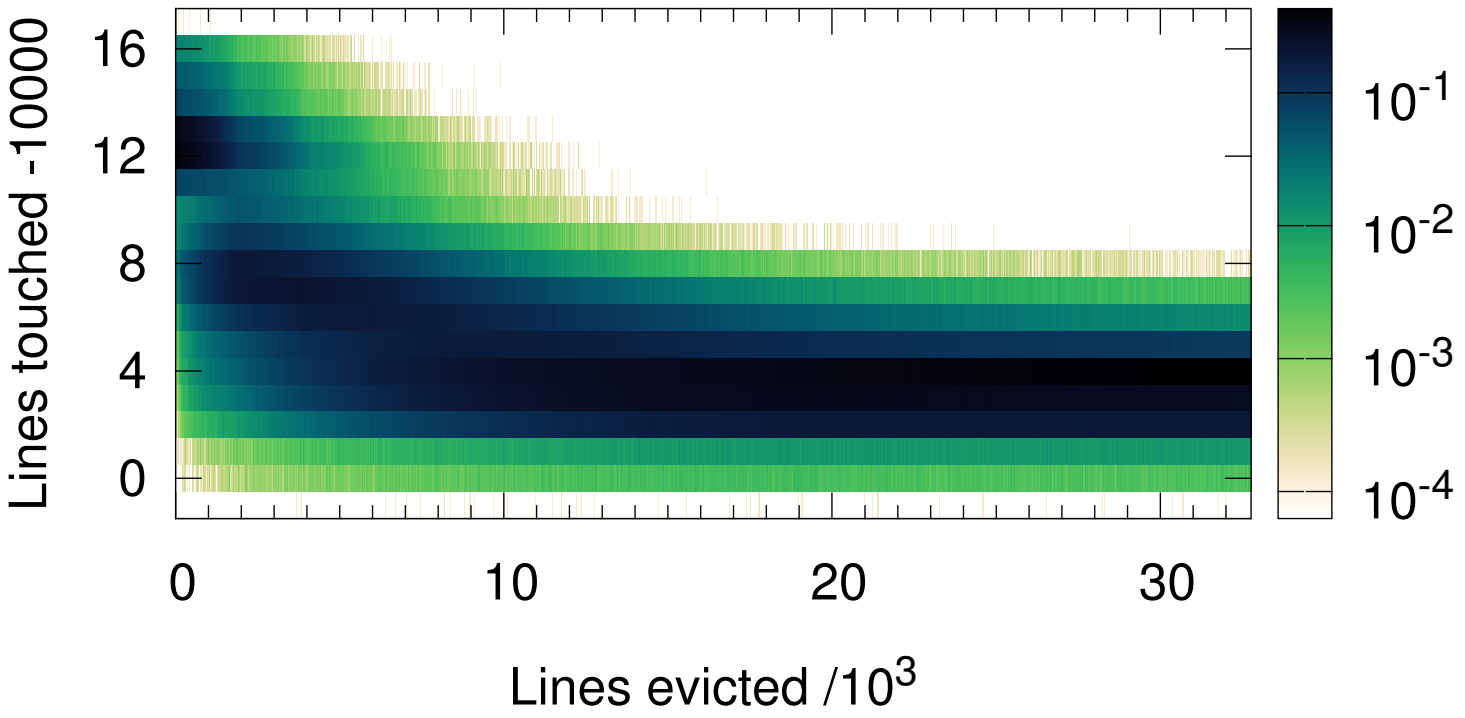
Exynos4412 Cache Channel with IBS



- Preempt after 10^5 instructions. Bandwidth: 400b/s.
- $6\times$ reduction — very poor result.
- Event delivery is imprecise thanks to speculation.

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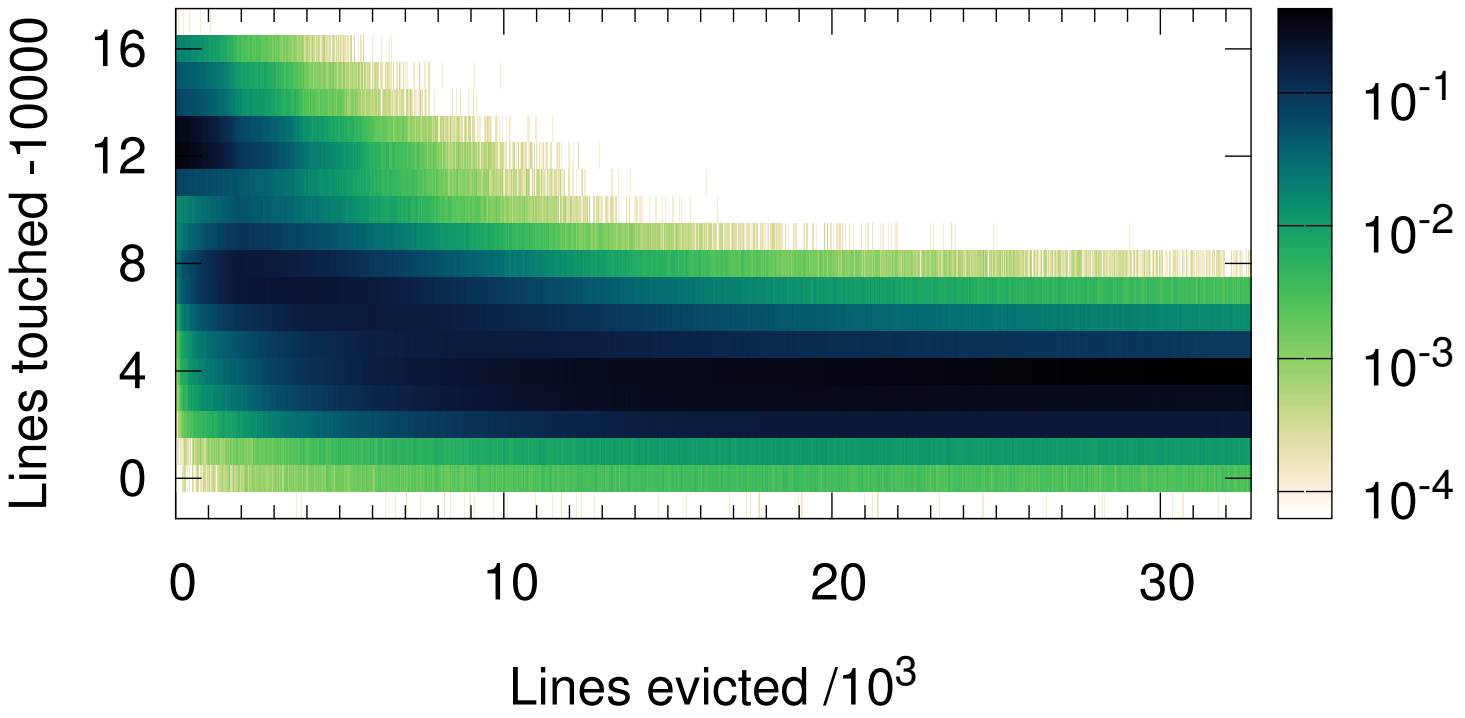

- Preempt after 10^5 instructions. Bandwidth: 400b/s.
- 6× reduction — very poor result.
- Event delivery is imprecise thanks to speculation.
- Attacker can modulate it!

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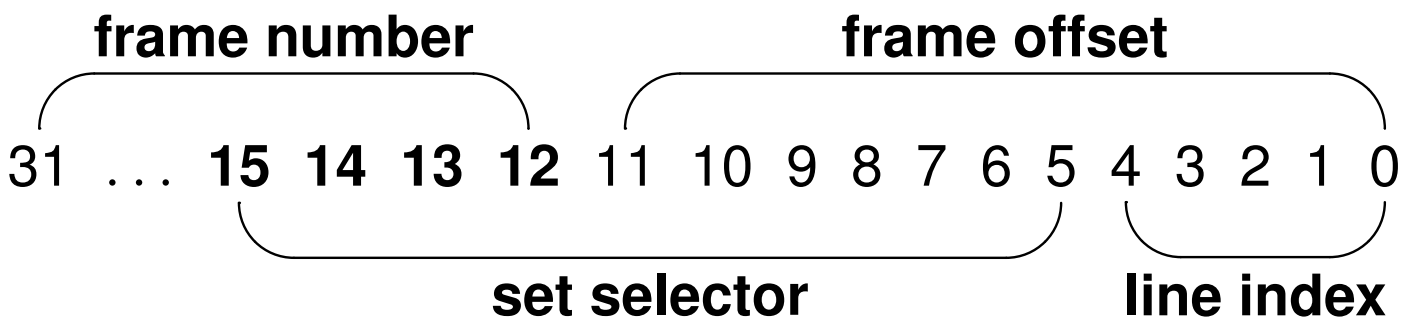
What is Colouring?



- Caches are divided into **sets** by **physical address**.

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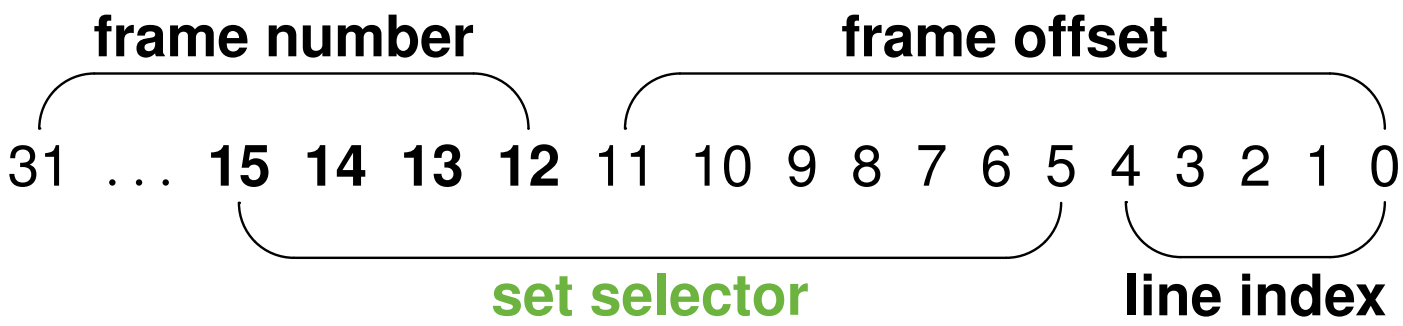

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- The **set selector** bits of the address choose the set.

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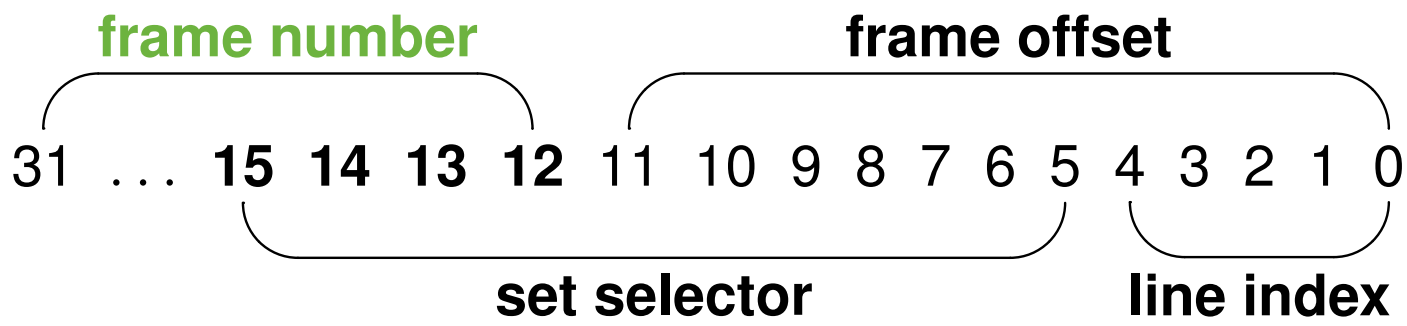

- Caches are divided into **sets** by **physical address**.
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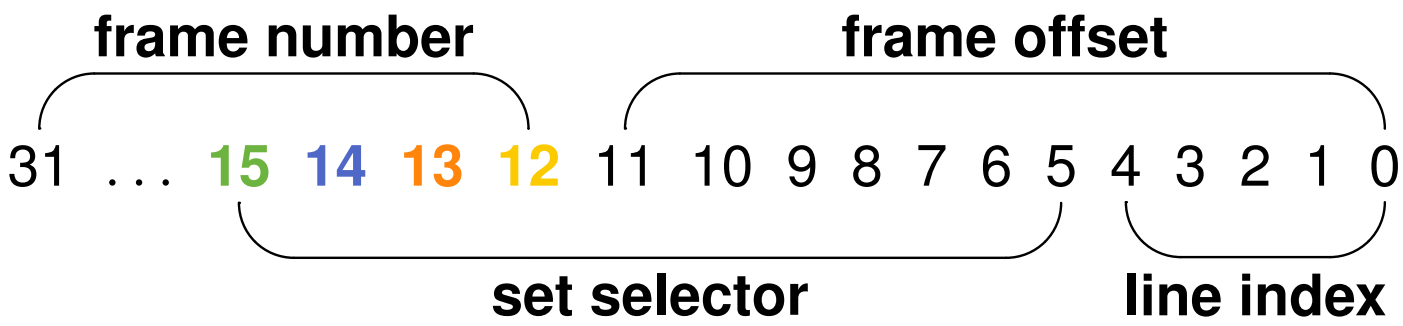

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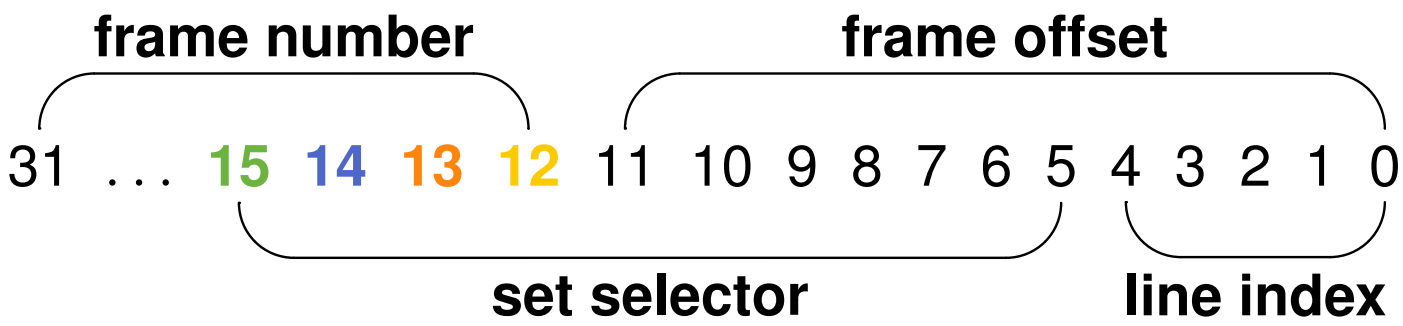

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- If these **colour bits** differ, the frames cannot collide.
- The frame number (phys. addr.) is **under OS control**.

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Colouring in seL4

In seL4, resource allocation is securely delegated. The initial task splits RAM in to coloured **pools**.

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- Low overhead.

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Advantages

- Very few kernel changes (in seL4).
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Disadvantages

- Only applies to the cache channel.
- Relies on internal details of cache operation.
- Doesn't work with large pages.
- Hashed caches break everything.

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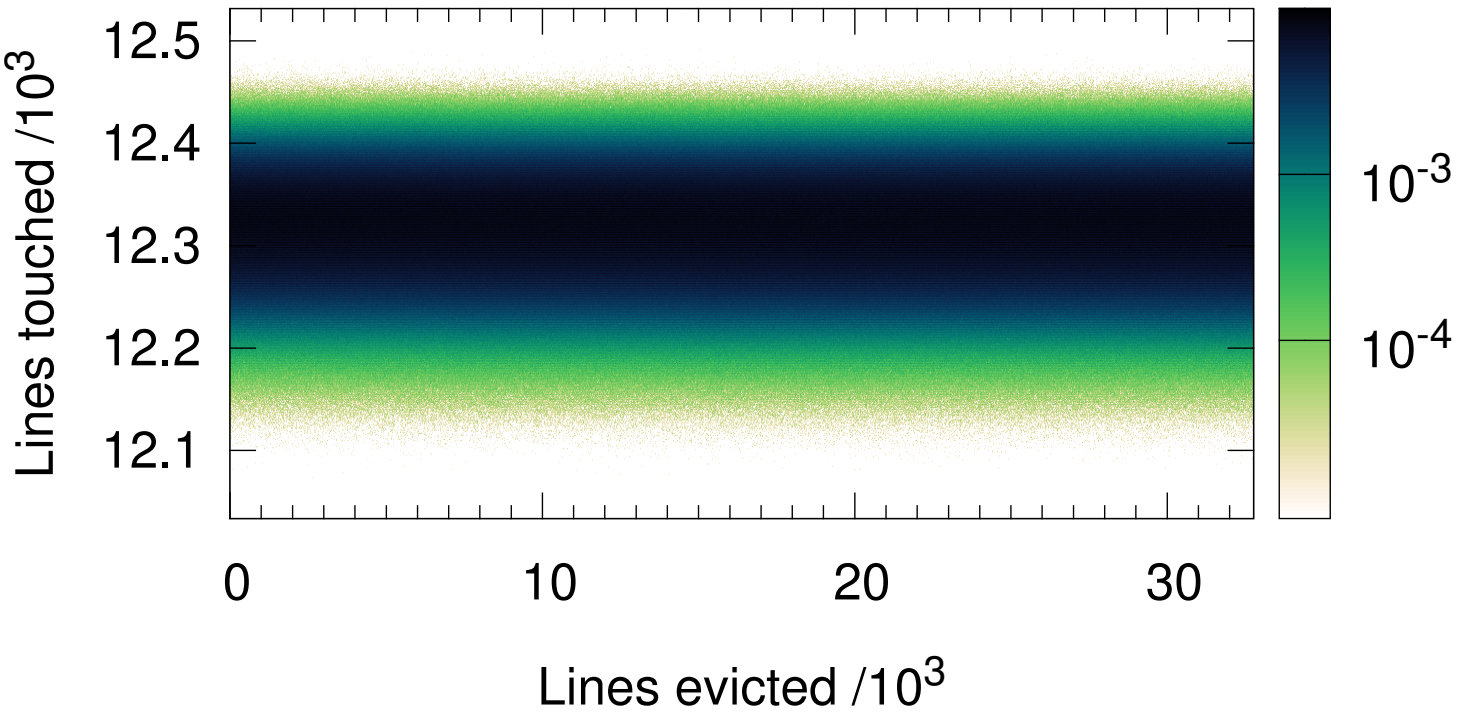
Exynos4412 Cache Channel, Partitioned



- Bandwidth: 15b/s.
- 160× reduction — Much better, but not perfect.

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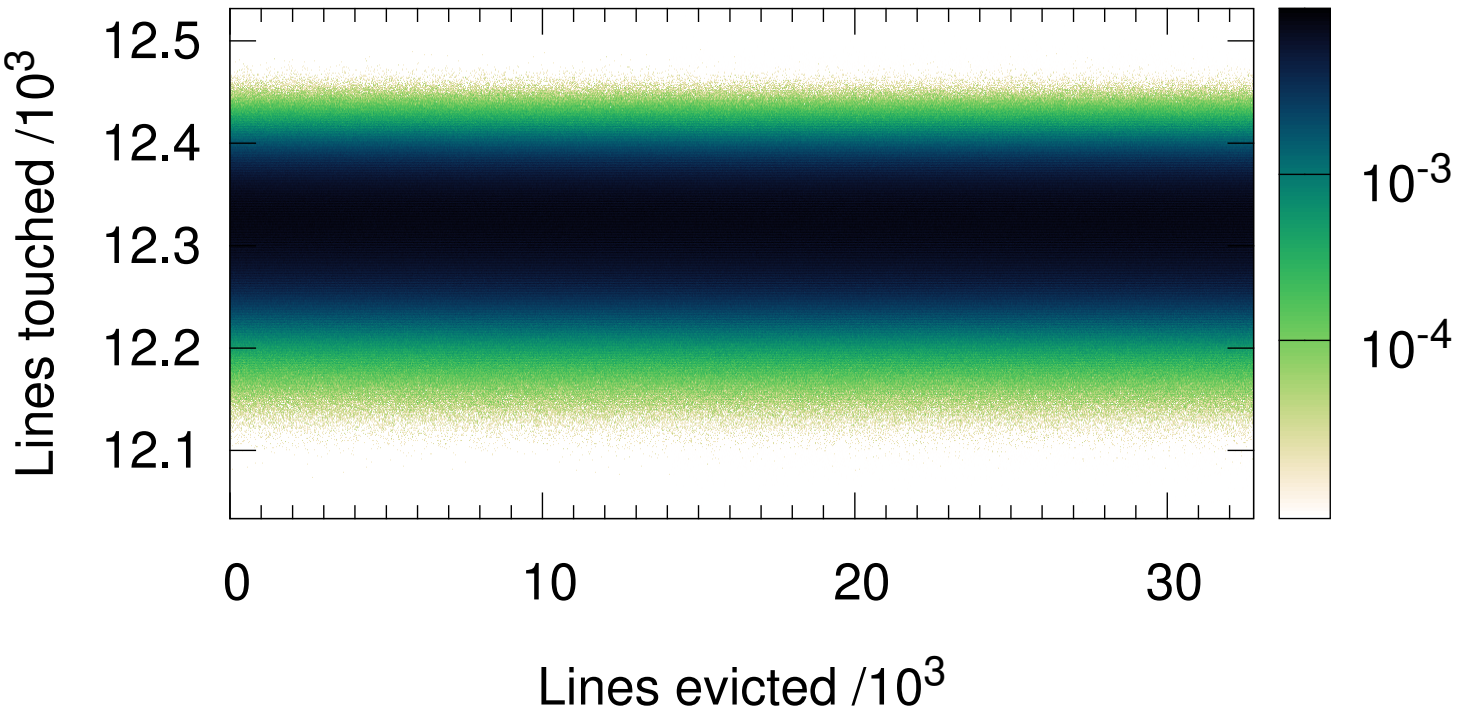

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Where does that 15b/s come from?

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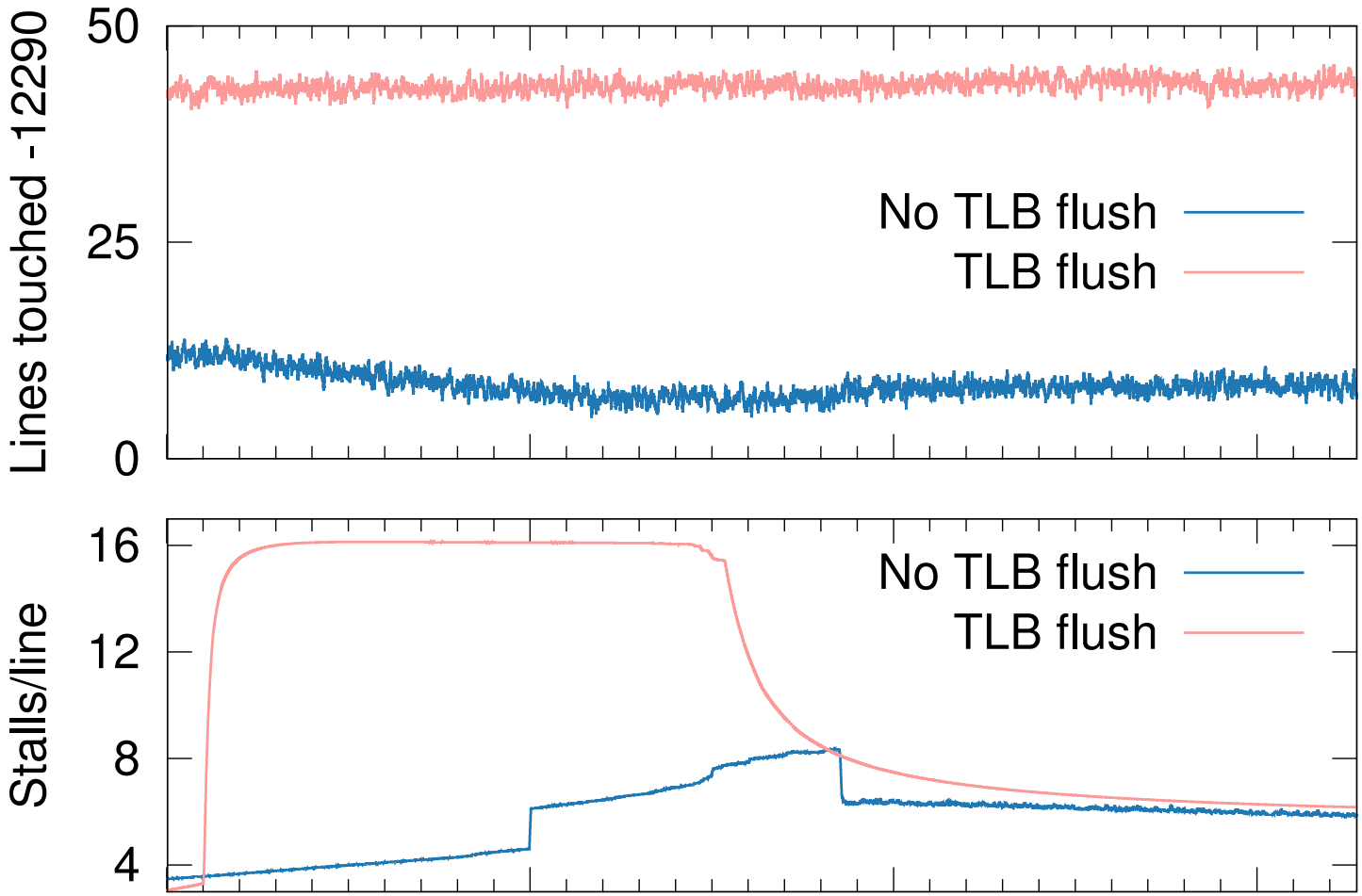
Exynos4412 TLB Channel



- Average rate correlates with TLB misses.
- Flushing on switch removes the signal.

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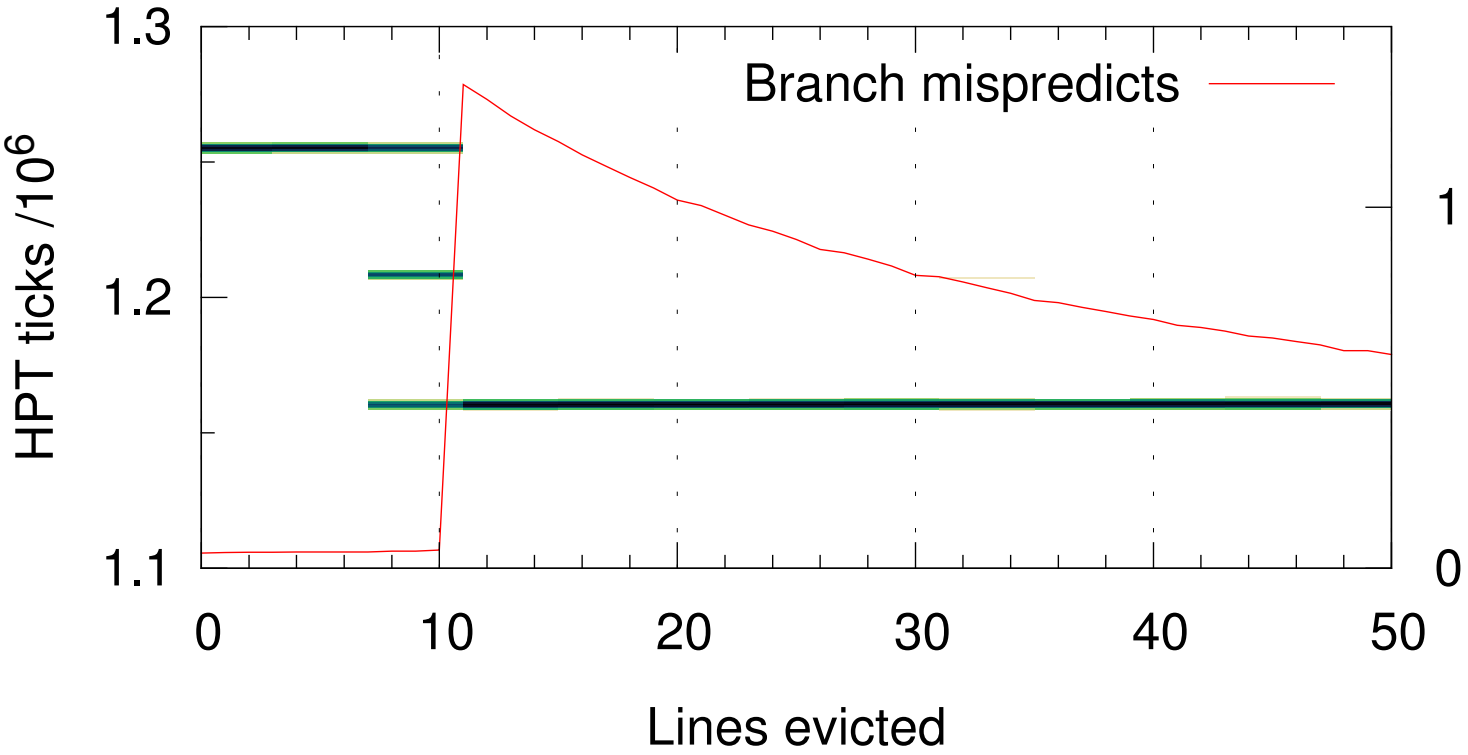
Misprediction and the Cycle Counter



- Cycle counter affected by invisible mispredicts.
- A new (an **unexpected**) channel.
- Event delivery is **precise**, the cycle counter is wrong.

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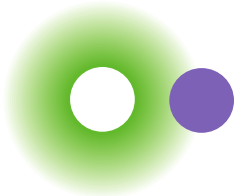

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The Lucky-13 Attack on TLS

Al Fardan & Paterson, SSP 2013

- Exploits non-constant-time MAC calculation.
- This is an **Algorithmic side-channel**.
- **Remotely exploitable**.
- We reproduce the distinguishing attack.

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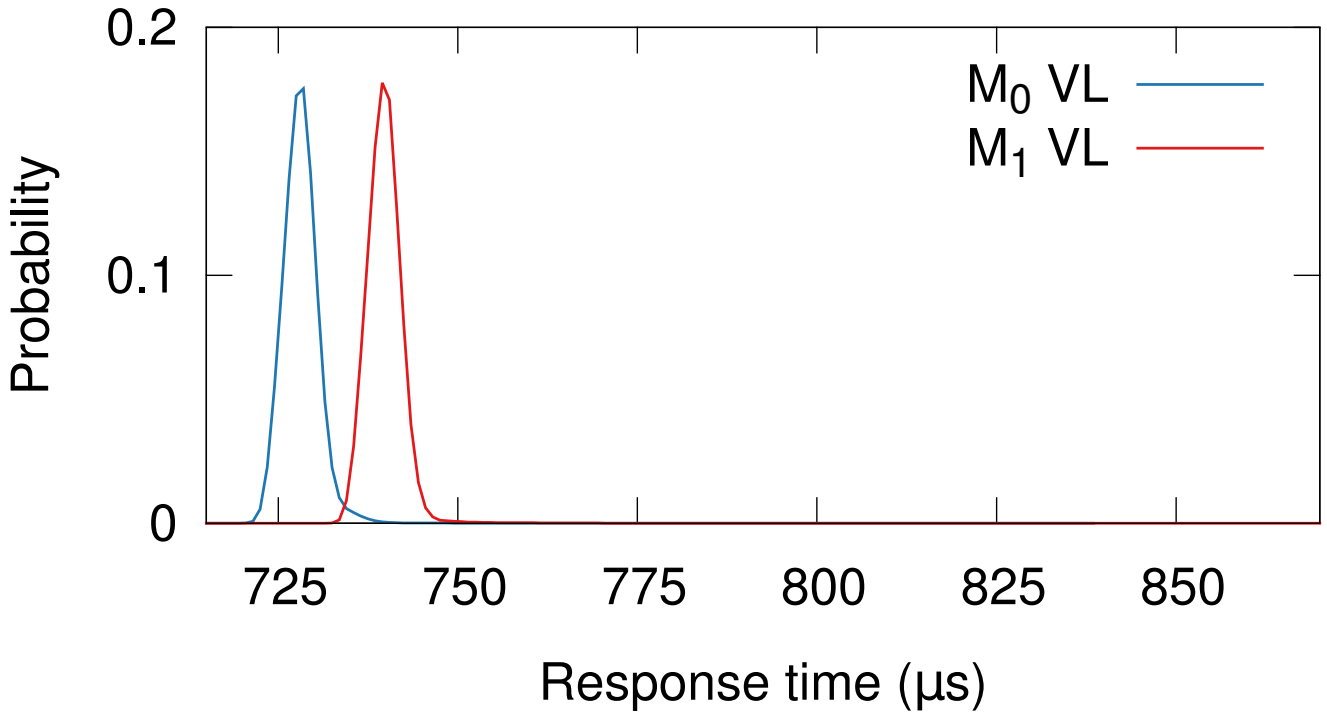
OpenSSL 1.0.1c Response Times



- Nearby attacker (crossover cable).
- Modified vs. unmodified packet.
- Distinguishable with $\approx$ 100% probability.

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The Upstream Fix: Constant-Time Code

Fixed in OpenSSL version 1.0.1e

A constant-time padding/MAC check.

- Now secure (on x86).
- We tested on ARM — still a small channel.

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The Upstream Fix: Constant-Time Code

Fixed in OpenSSL version 1.0.1e

A constant-time padding/MAC check.

- Now secure (on x86).
- We tested on ARM — still a small channel.
- We present an OS-level solution, with:
  - Better performance.
  - Lower latency.
  - Lower CPU overhead.
  - No modification of OpenSSL.

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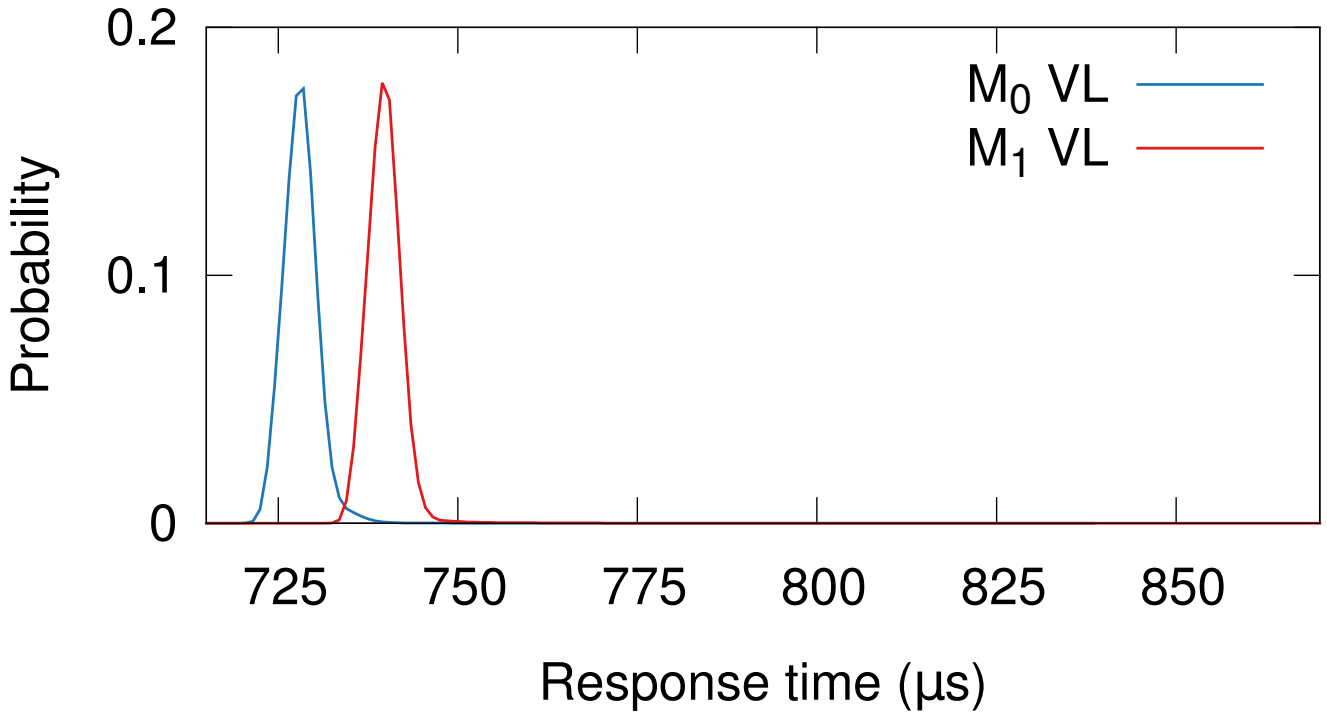

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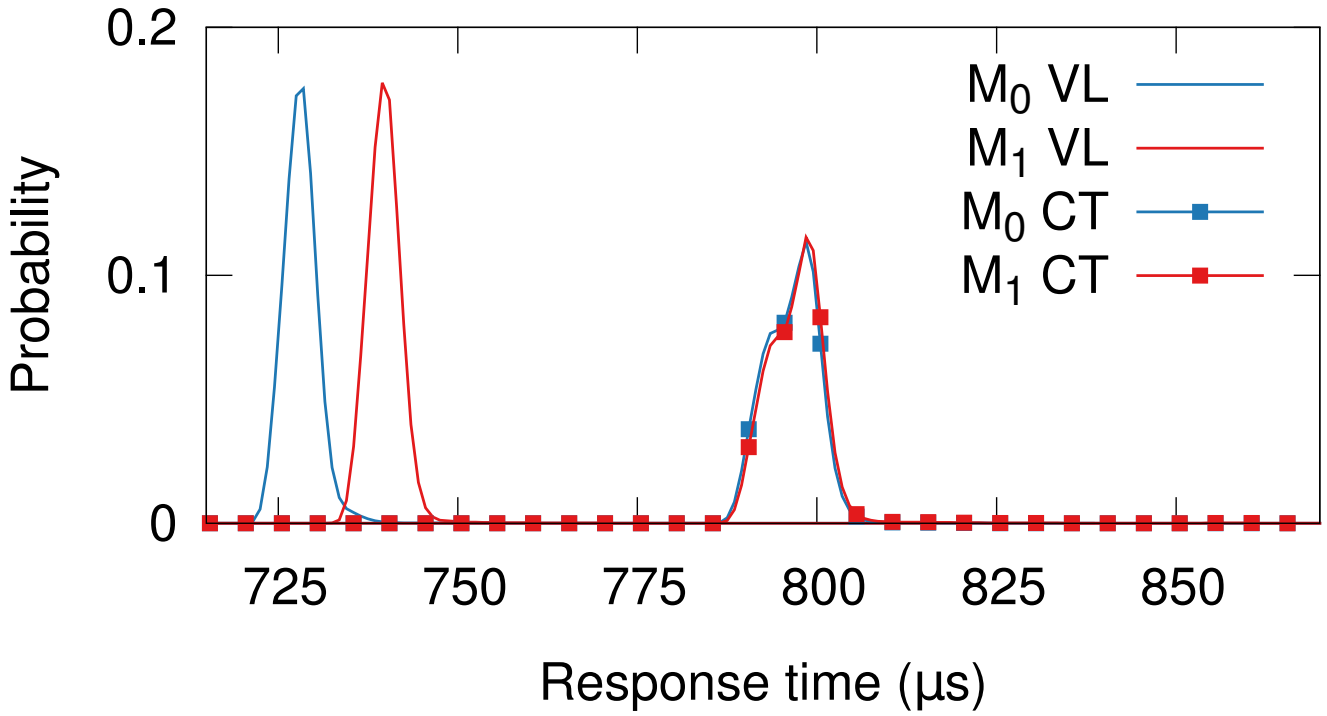

- Constant-time implementation.
- Better, but still distinguishable — 62%.
- 60μs (8.1%) latency penalty.

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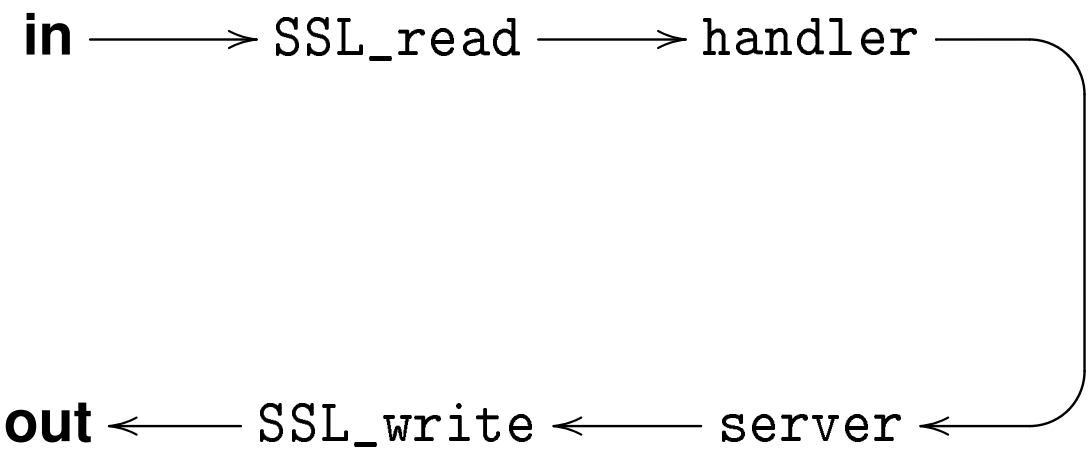

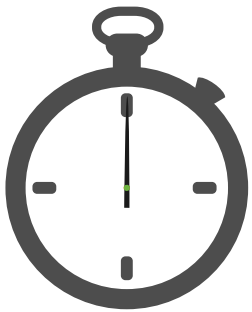

- Separate OpenSSL and application.
- Announce packets over IPC.

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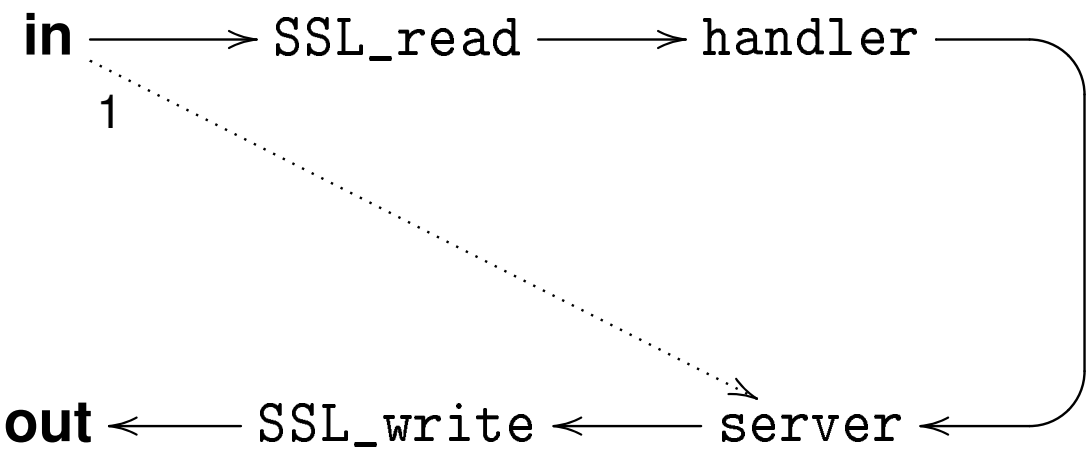

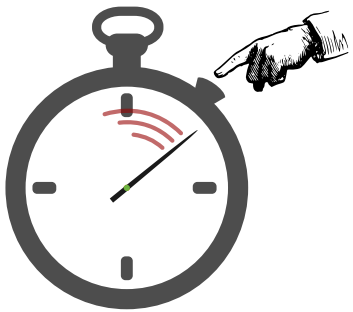

- Separate OpenSSL and application.
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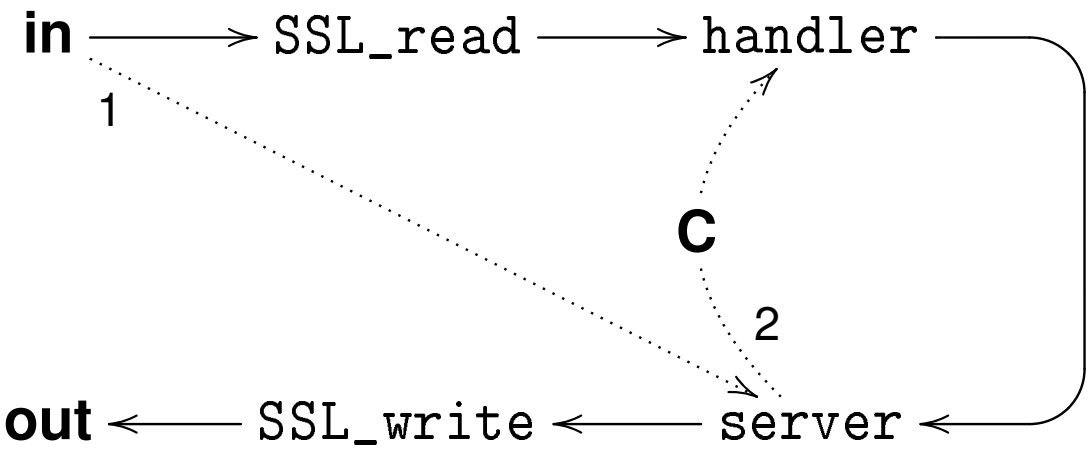

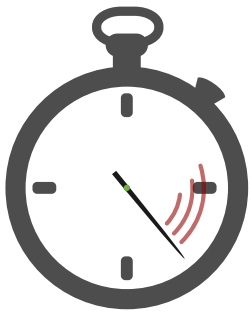

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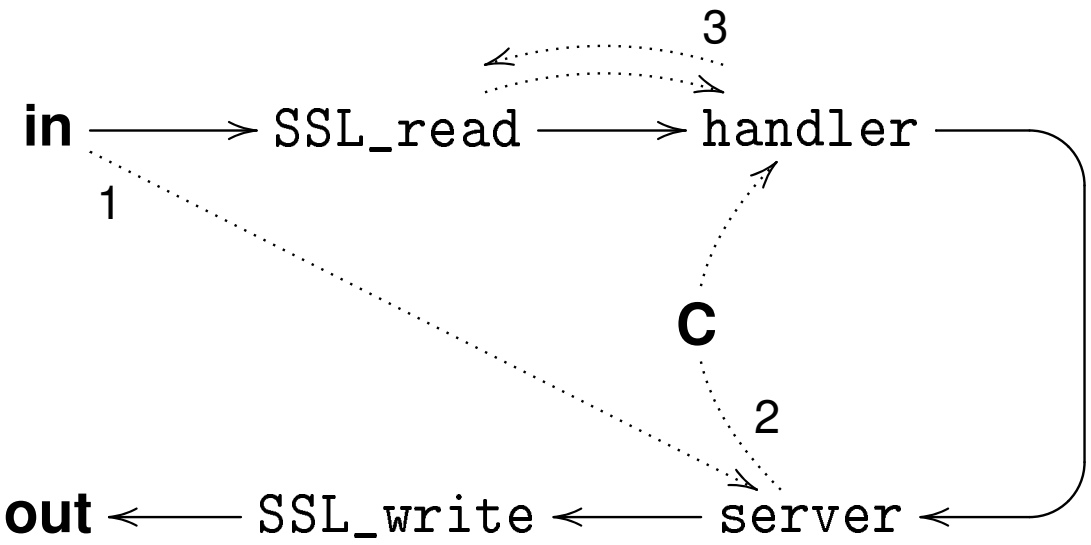

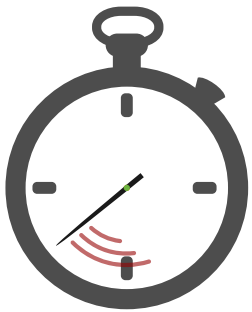

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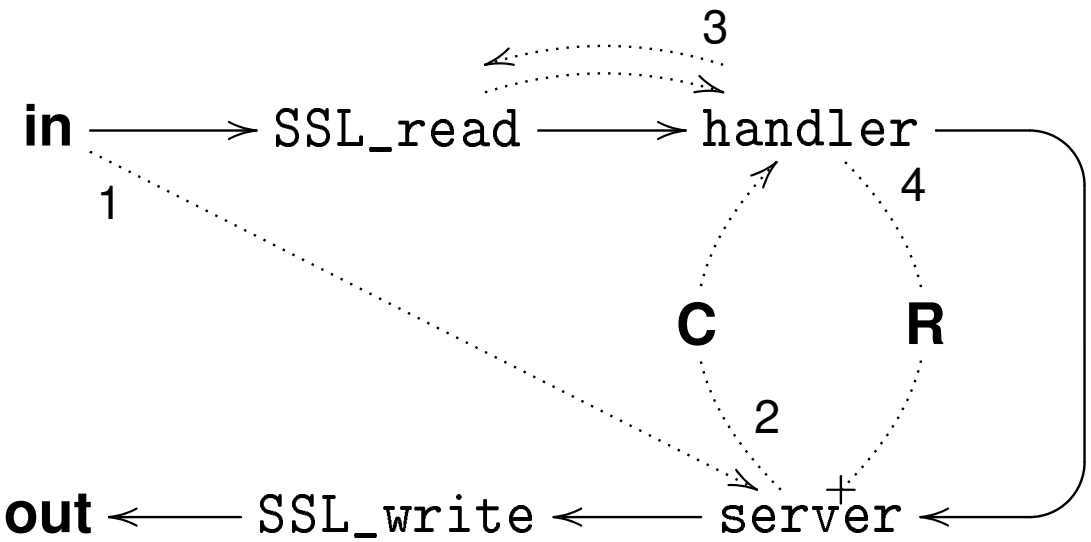

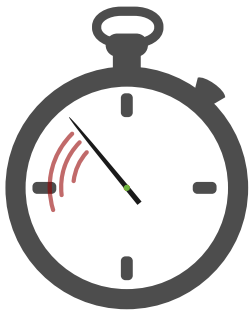

- Separate OpenSSL and application.
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- Record arrival time.
- Block response on timer.

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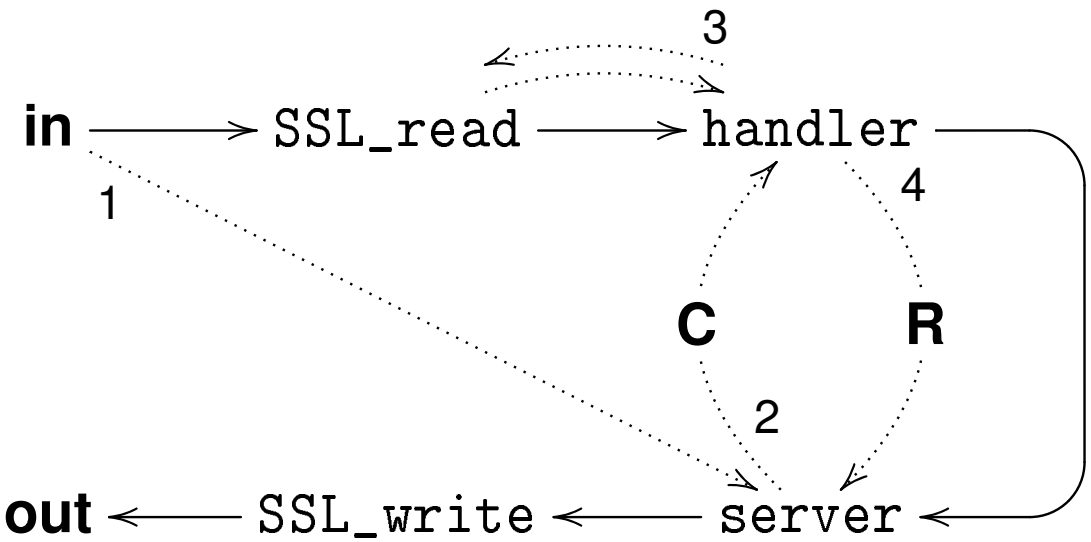

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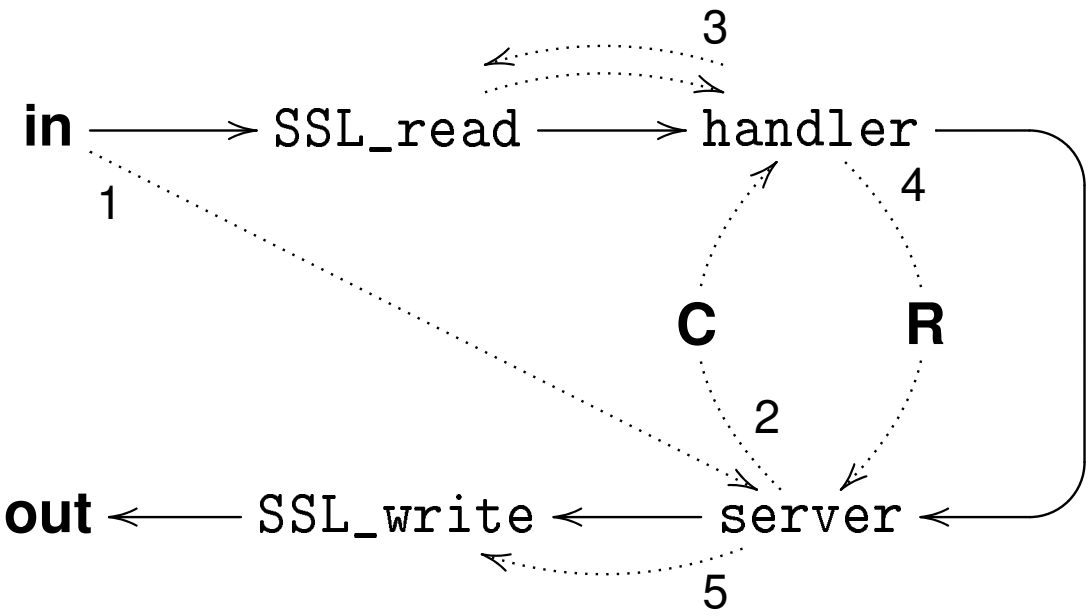

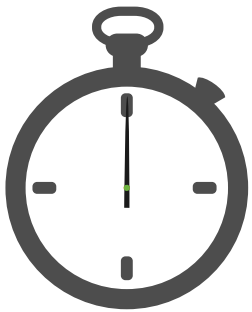

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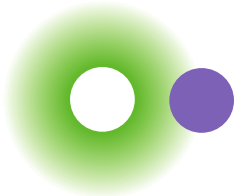
Scheduled Delivery on seL4



We use **real-time scheduling** to precisely delay messages.
Provides an efficient **mechanism** to enforce a delay **policy**:
See *Askarov et. al., CCS 2010*.

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Advantages

- Uses existing IPC controls — no modifications.
- Fast and effective (see next slide).

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Provides an efficient **mechanism** to enforce a delay **policy**:
See *Askarov et. al., CCS 2010*.

Advantages

- Uses existing IPC controls — no modifications.
- Fast and effective (see next slide).

Disadvantages

- Specific to remote/network attacks.
- Need to wrap (but not modify) vulnerable component.

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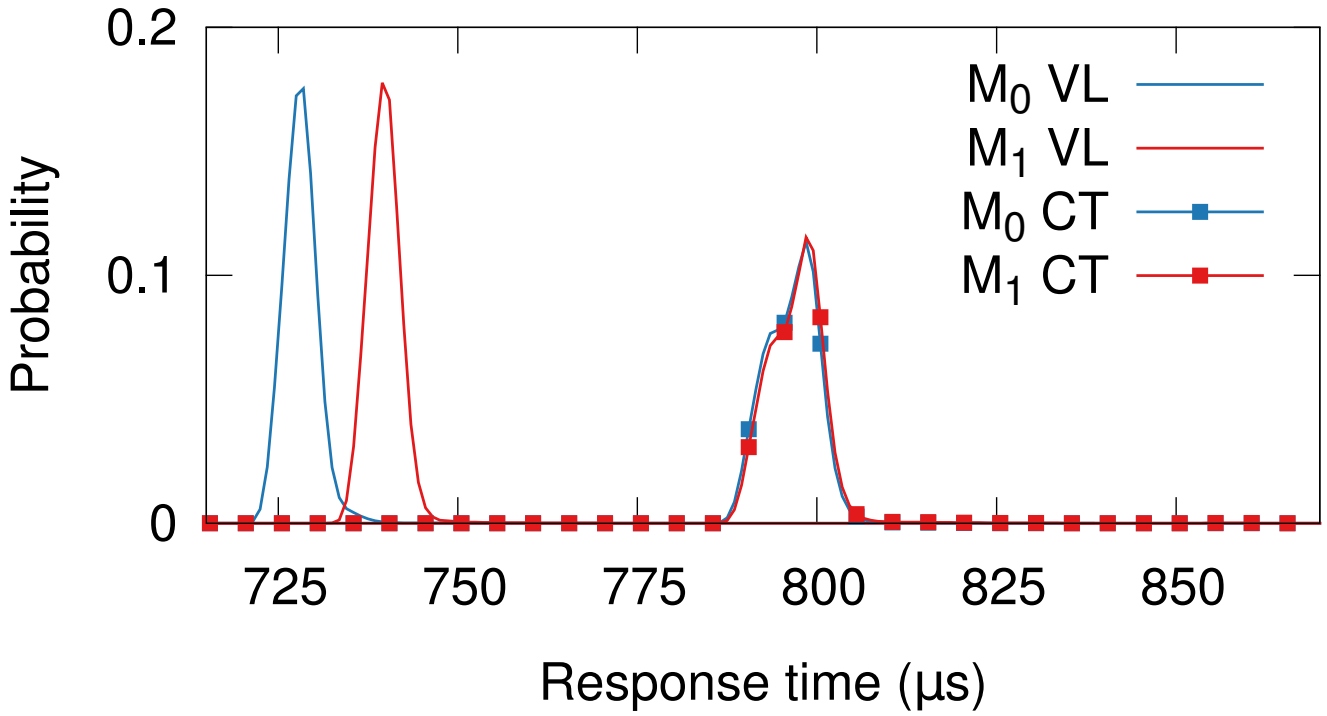
Security of Scheduled Delivery



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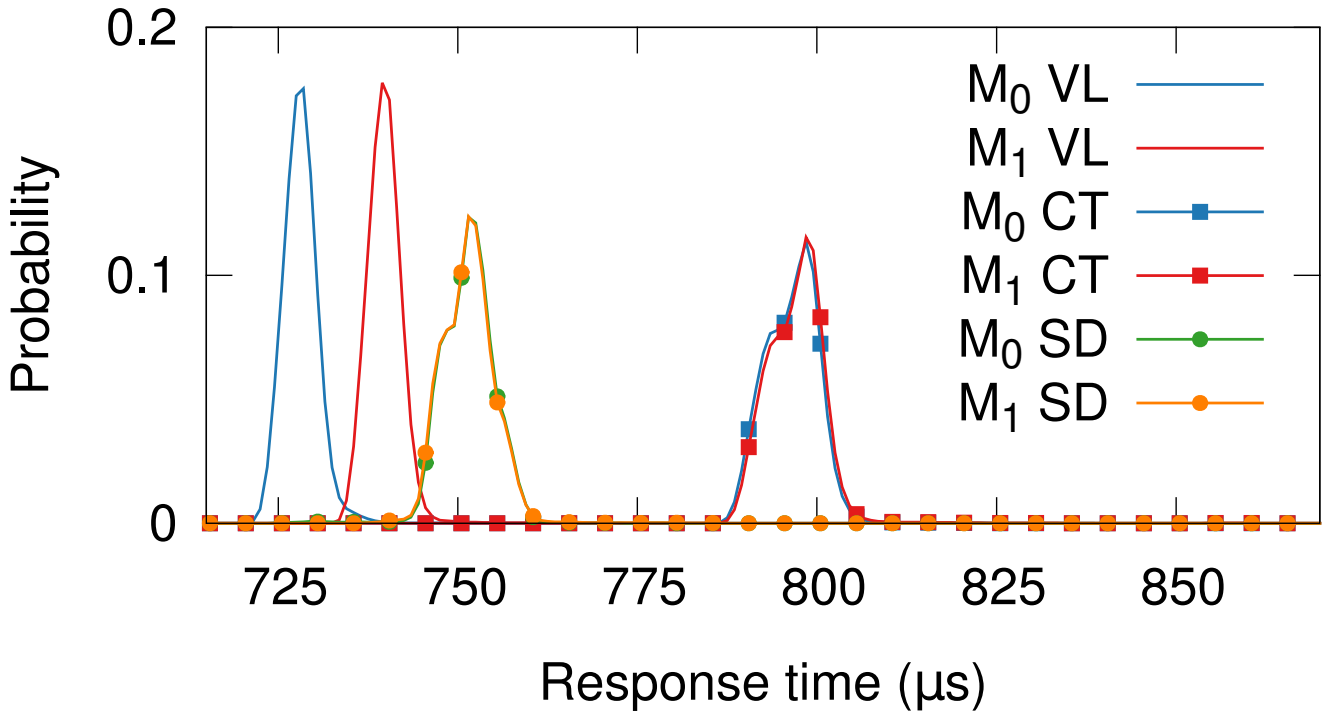

- More secure — 57% distinguishable.
- Faster — 10μs (1.4%) latency penalty.

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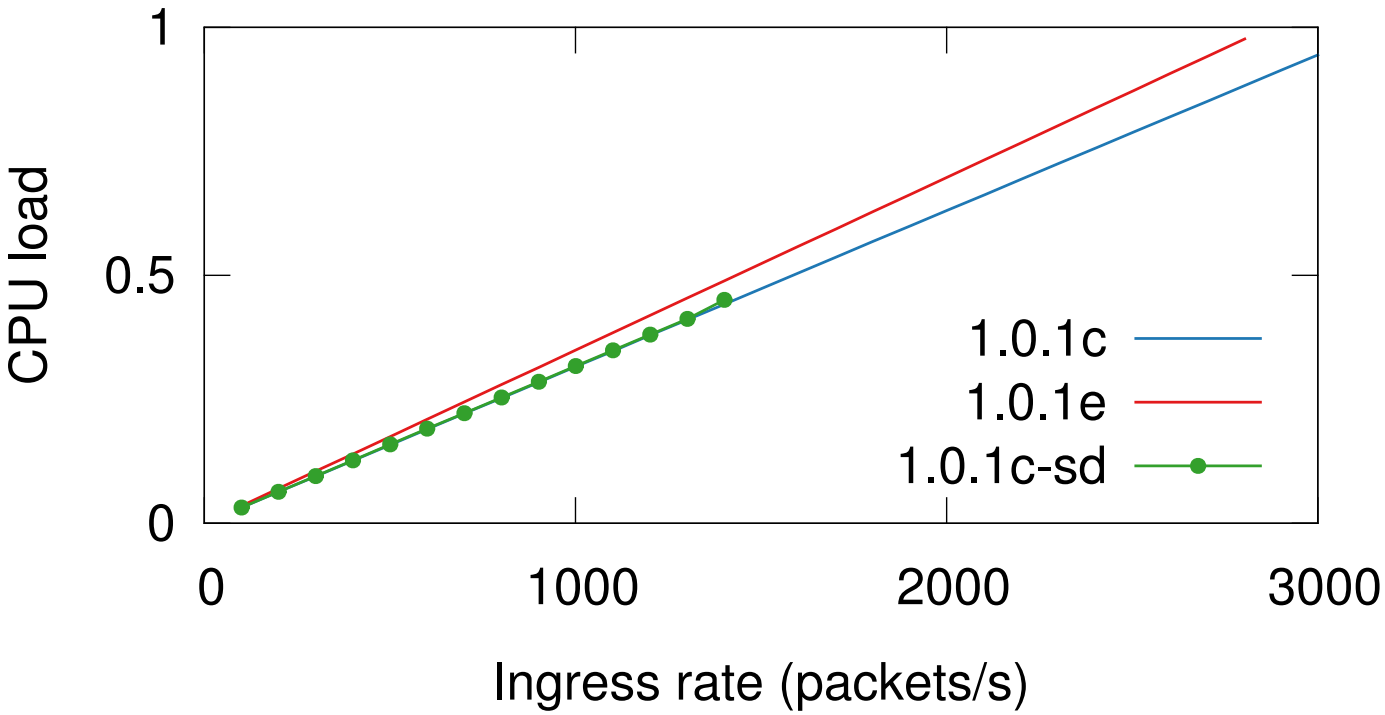
Performance of Scheduled Delivery



- Lower overhead (2% vs. 11%), but earlier saturation.
- This is a worst-case benchmark — no server work.

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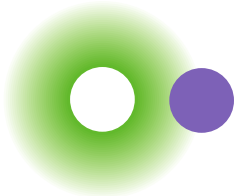

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Outcomes

These channels are real

- We managed to exploit every channel we tried.
- The bandwidth is high, and growing.

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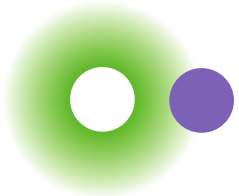

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They're getting worse

- Countermeasures get less effective on newer chips.
- New hardware channels e.g. branch predictor.

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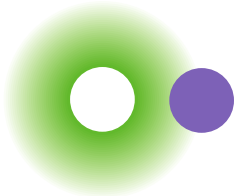

These channels are real

- We managed to exploit every channel we tried.
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They're getting worse

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But there is hope

- Resource partitioning (e.g. colouring) is effective.
- Repurpose hardware QoS features.
- OS-level techniques can help.

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Ongoing Work

- Ongoing project at NICTA (Qian Ge).
- Developing a fully cache-coloured seL4.
- We use these tools to evaluate the result.

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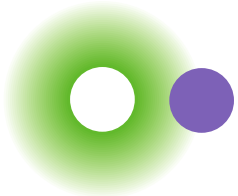

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Questions?

Data and Tools `http://ssrg.nicta.com.au/projects/TS/timingchannels.pml`

seL4 Is Open Source! `http://sel4.systems`

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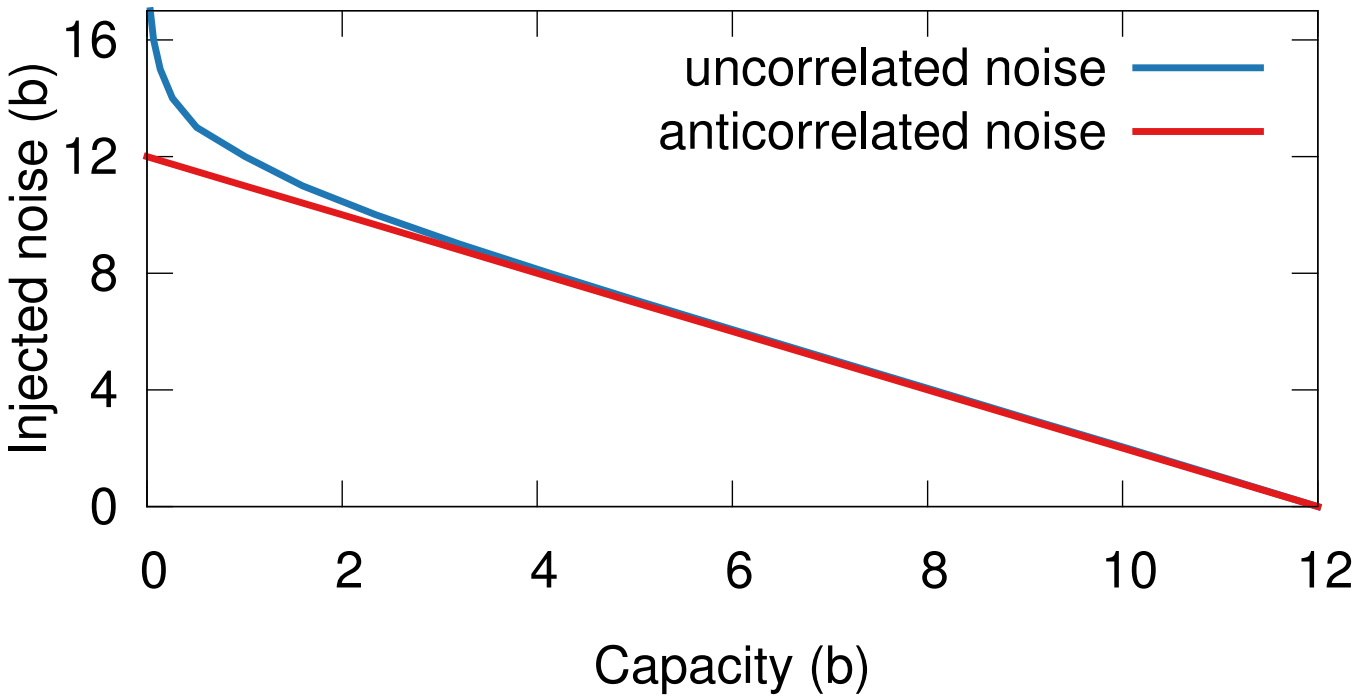
Capacity vs. Injected Noise



- Noise injection doesn't scale.
- Increasing determinism is the way to go.

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